REVIEW OF LOGIC DEVICES

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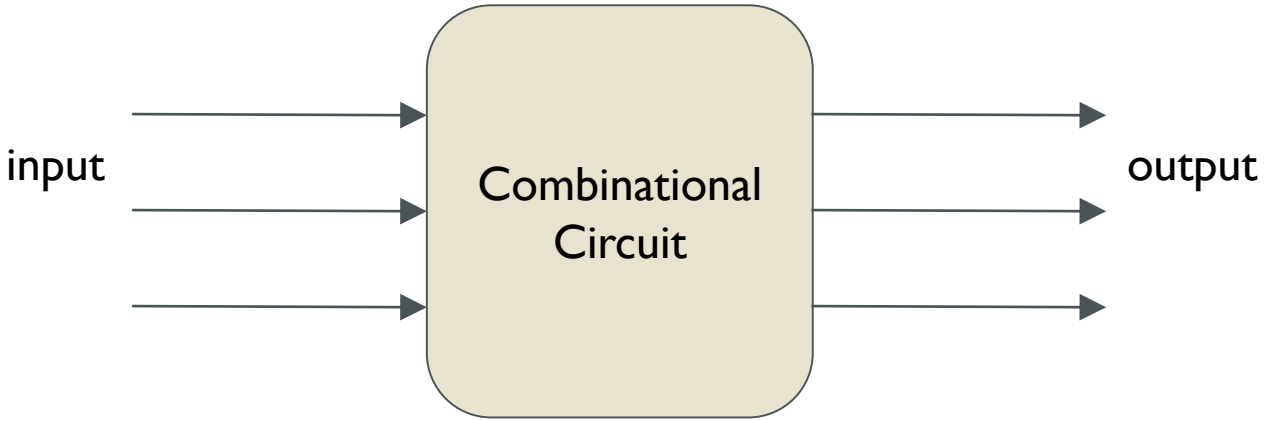
Target Audience : 5th Semester Students

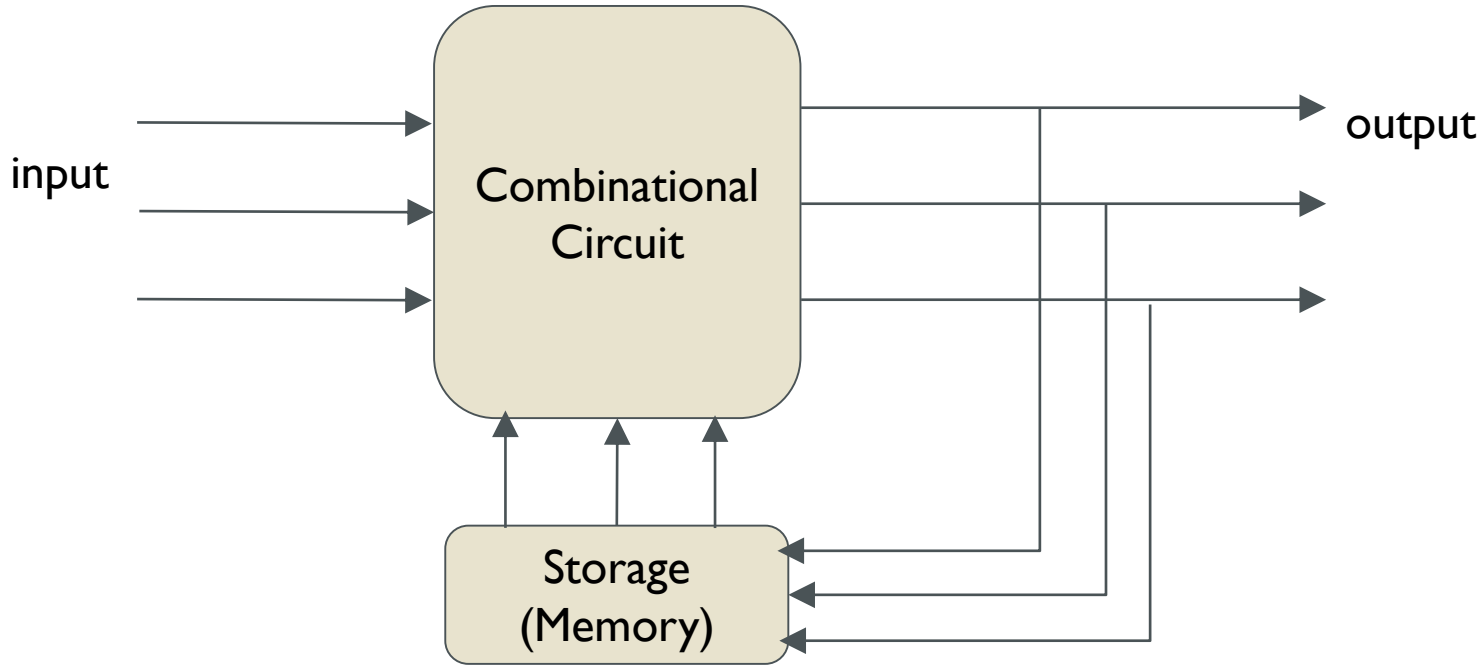
LEARNING OBJECTIVES

- Understand difference between combinational circuits and sequential circuits
- Understand basic S-R latch
- Understand different types of flip-flops
- Buffers and Controlled Buffers
- Registers
- Decoders and Encoders

COMBINATIONAL CIRCUITS



SEQUENTIAL CIRCUITS



- ➔ It is important that any meaningful circuit, any design, any hardware, any system have to necessarily contain sequential circuits if you want to have a behaviour pattern as per a sequence of events.
- ➔ A storage element is required. (Memory)

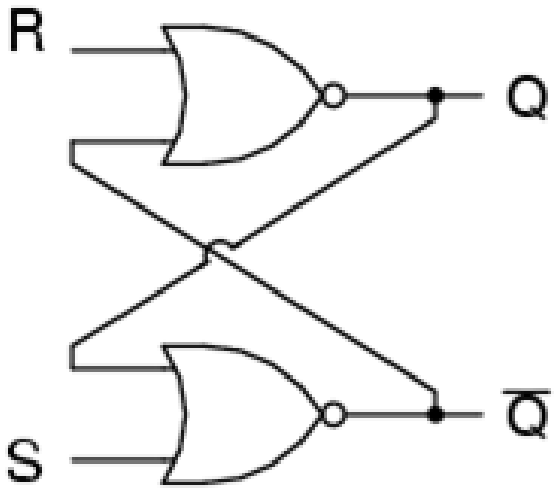
REQUIREMENT OF MEMORY

- If stored data is 0, it must remain 0 as long as it is possible.
- If stored data is 1, it must remain 1 as long as possible.

LATCH

➔ A basic storage element is called latch.

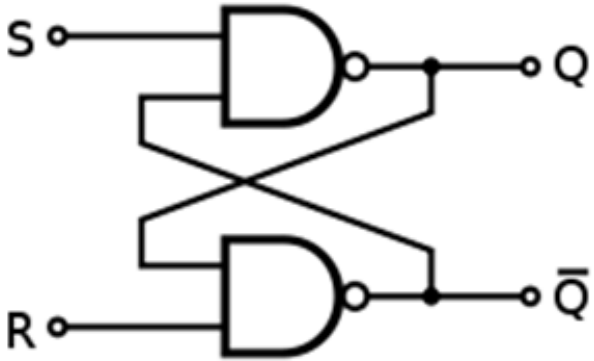
Characteristics Table of S-R Latch using NOR Gate			
S	**R**	Q	$\overline{Q}$
0	0	Memory (as before)	
0	1	1	0
1	0	0	1
1	1	Not used	



S – R Latch using NOR Gate

LATCH

Characteristics Table of S-R Latch using NAND Gate			
S	**R**	Q	$\overline{Q}$
0	0	Not used	
0	1	0	1
1	0	1	0
1	1	memory	



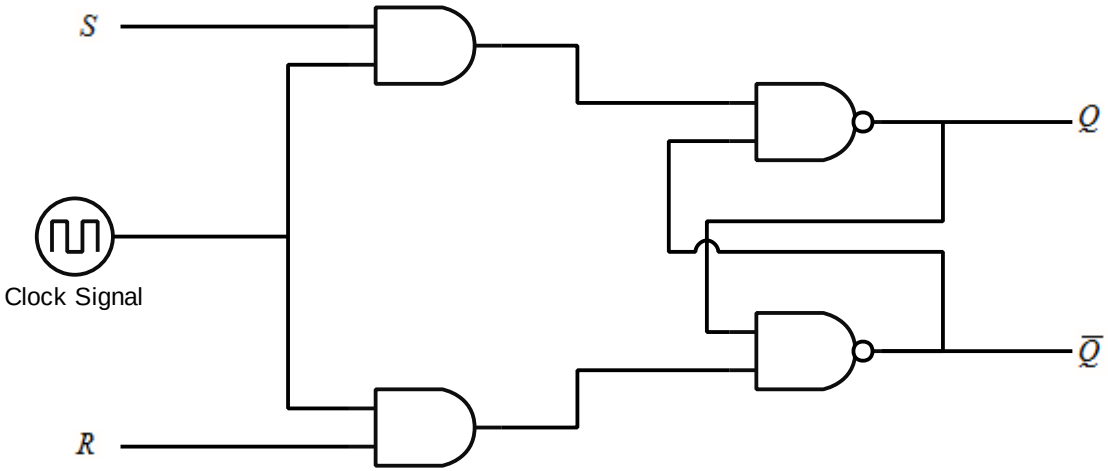
S – R Latch using NAND Gate

FLIP-FLOP

- When clock signal is introduced in Latch, it is called Flip-Flop.
- Clock signal is High
  - ➔ S & R combination will change the output.
- Clock signal is Low
  - ➔ S & R combination will not change the output.
  - ➔ Memory is retained.

S – R FLIP-FLOP

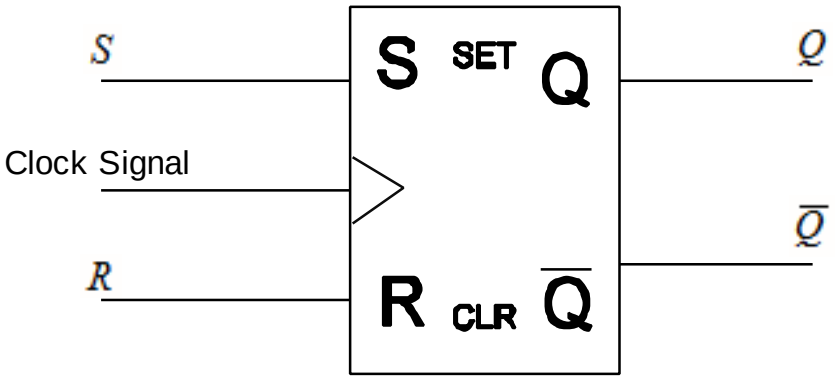
Characteristics Table of S-R Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
0	X	X	Memory	
I	0	0	Memory	
I	0	I	0	I
I	I	0	I	0
I	I	I	Not used	



Logic Diagram of S – R Flip-Flop

S – R FLIP-FLOP

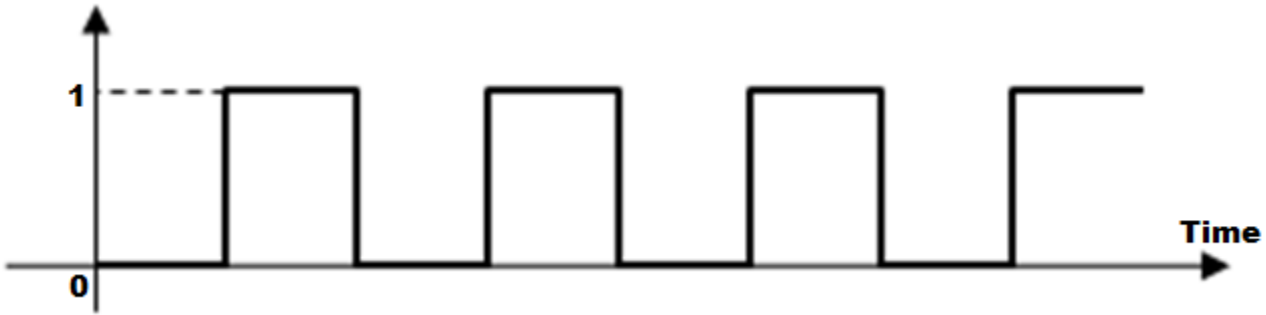
Characteristics Table of S-R Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
0	X	X	Memory	
I	0	0	Memory	
I	0	I	0	I
I	I	0	I	0
I	I	I	Not used	



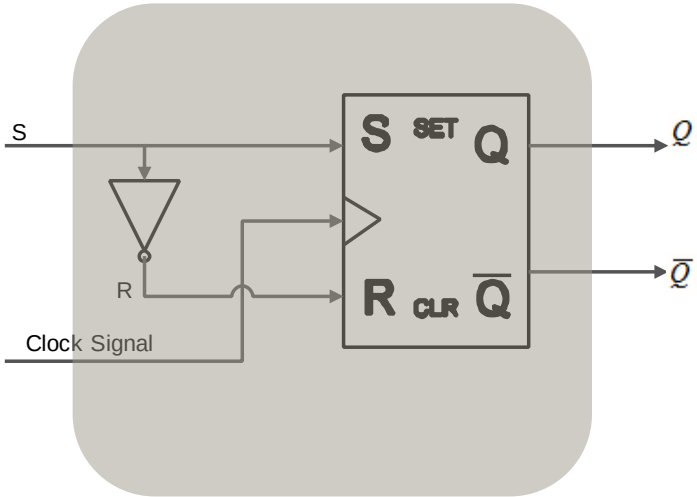
Symbol of S – R Flip-Flop

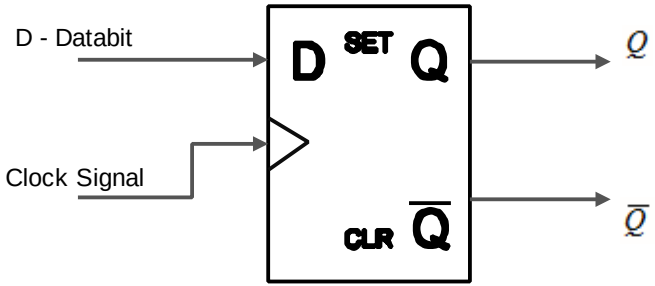
CLOCK SIGNAL

- What is Clock Signal ?
- Why do we need this clocking operation ?
- How to decide clock signal length ?



D FLIP-FLOP





Symbol of D Flip-Flop

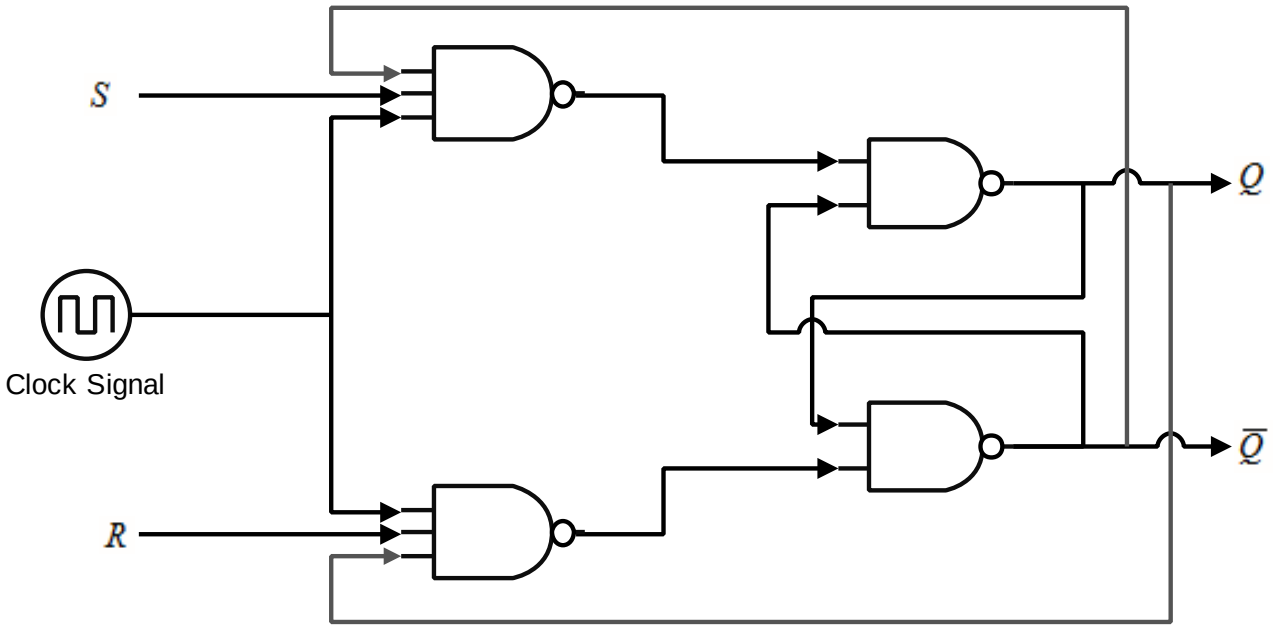
D FLIP-FLOP

Characteristics Table of S-R Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
0	X	X	Memory	
1	0	0	Memory	
1	0	1	0	1
1	1	0	1	0
1	1	1	Not used	

Characteristics Table of D Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
0	No change in Data Stored			
1	1	0	1	0
1	0	1	0	1

D FLIP-FLOP

- D Flip-Flop is one bit storage element.
- Used in Data Storage Device.

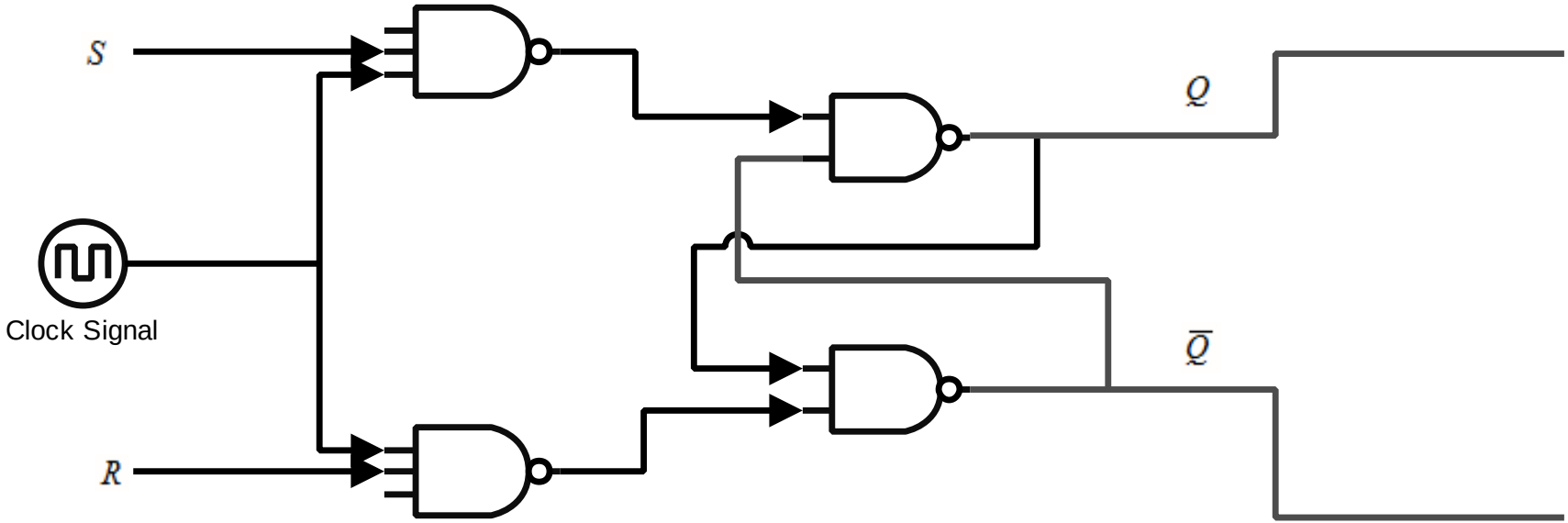

S
R
Clock Signal
Q
$\overline{Q}$

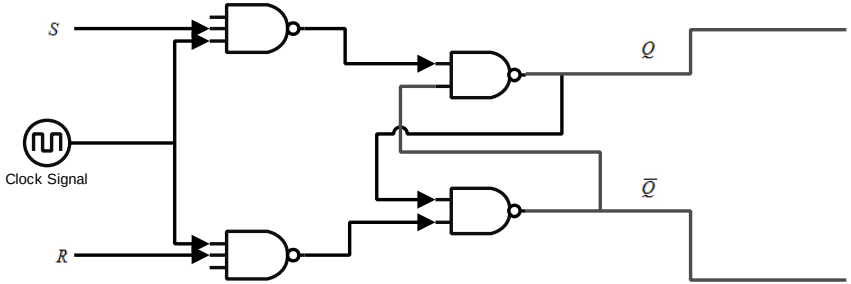
Characteristics Table of Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
1	1	0	1	0
1	0	1	0	1

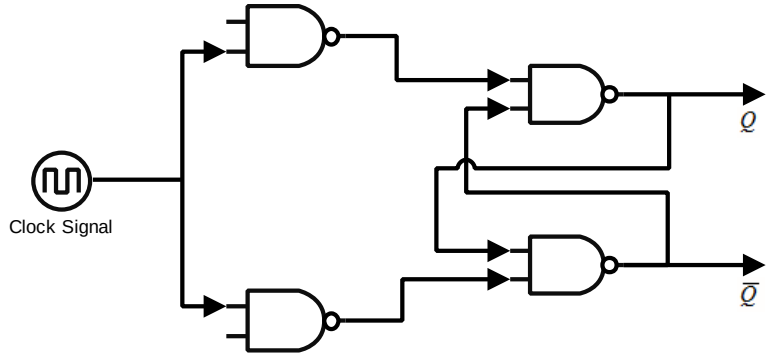
Characteristics Table of Flip-Flop				
Clock Signal	**S**	**R**	Q	$\overline{Q}$
1	1	1	1	0
			0	1
			1	0
			0	1
			1	0
			0	1
			1	0

Racing

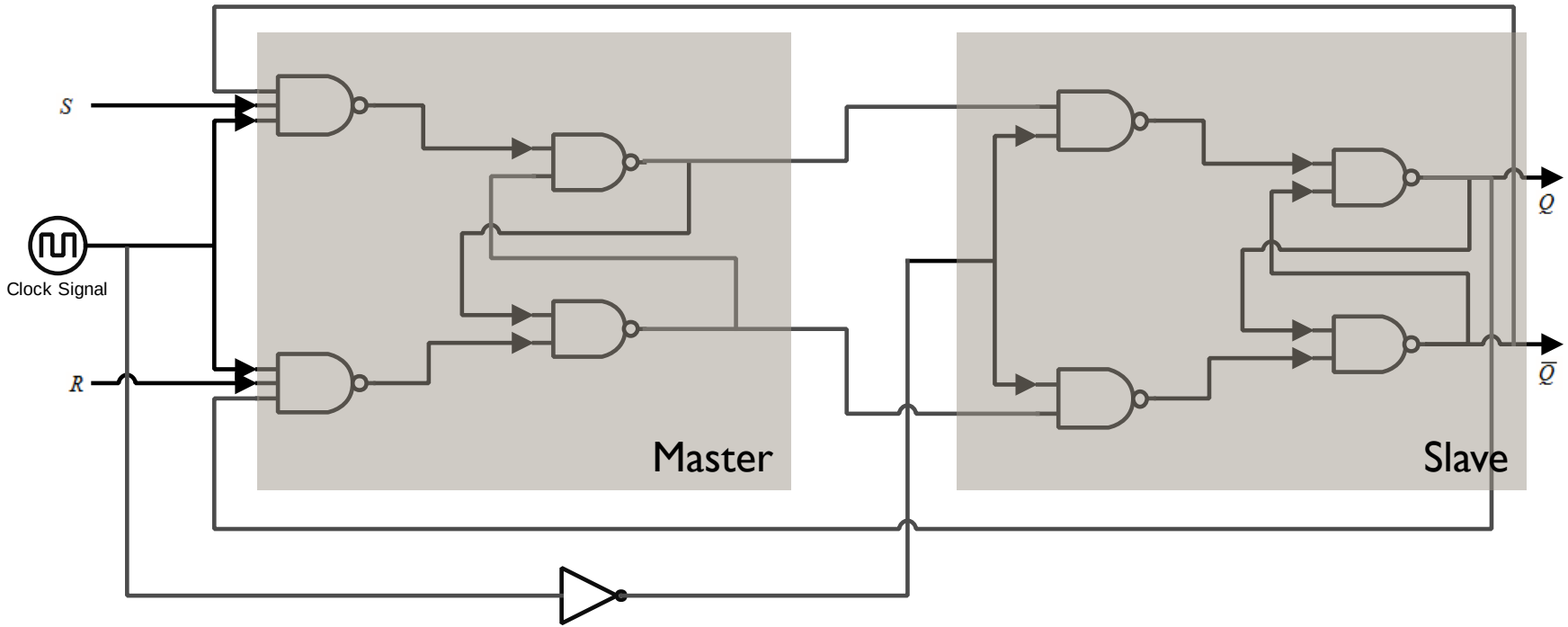
Depends on propagation delay of flip-flop


S
R
Clock Signal
Q
$\overline{Q}$


S
Clock Signal
R
Q
$\overline{Q}$


Clock Signal
Q
$\overline{Q}$

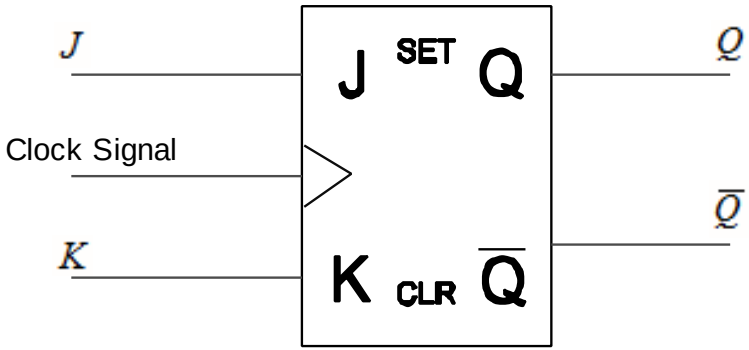
J-K FLIP-FLOP



Logic Diagram of J – K Flip-Flop

J-K FLIP-FLOP

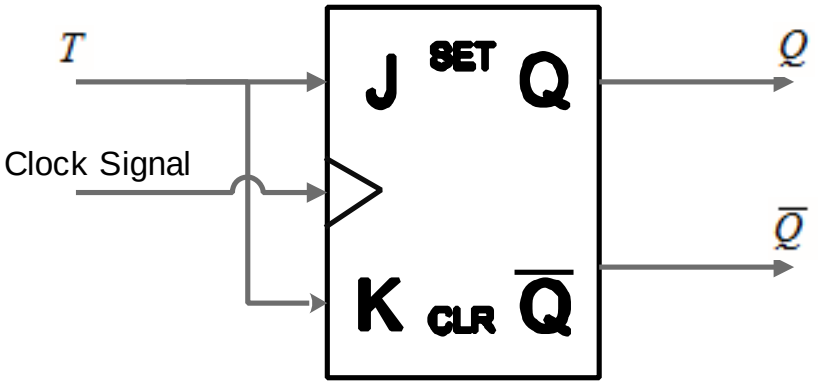
Characteristics Table of J-K Flip-Flop				
Clock Signal	**J**	**K**	Q_n	$\overline{Q_n}$
0	X	X	Memory	
I	0	0	Memory	
I	0	I	0	I
I	I	0	I	0
I	I	I	Q_{n-1}	$\overline{Q_{n-1}}$



Symbol of J-K Flip-Flop

T FLIP-FLOP

Characteristics Table of T Flip-Flop		
Clock Signal	**T**	Q_n
0	X	Q_{n-1}
I	0	Q_{n-1}
I	I	$\overline{Q_{n-1}}$



Symbol of T Flip-Flop

EDGE TRIGGERED FLIP-FLOP

- Level Triggered Flip-Flop
- Positive Edge Triggered Flip-Flop
- Negative Edge Triggered Flip-Flop

REQUIRED RESOURCES

- ✓NPTEL (National Program on Technology Enhanced Learning)
- ✓Scilab (Open Source Software)
- ✓Apache Open Office (Open Source Software)
- ✓Wikipedia (Free Online Encyclopaedia)
- ✓Google Slides (Open Source Application)
- ✓Google Drawings (Open Source Application)